

### **Rejection under 35 U.S.C. §112**

Claim 3 has been rejected under 35 U.S.C. §112, second paragraph, since the Examiner indicates a lack of knowledge as to where in the drawings it is shown that a capacitor is provided connected between two neighboring conductors.

As explained under “Objections to the drawings”, the previously mentioned feature of claim 3 in connection with a capacitor is shown in Fig. 4.

### **Claim Rejection under 35 U.S.C. §102**

Claims 1-3 and 7 have been rejected under 35 U.S.C. §102(b) as being anticipated by IBM Technical Disclosure Bulletin No. 85046791.

Claim 1 provides that capacitors are electrically connected to at least one surface of conductors, each of the conductors being electrically connected to either one of power supply connection pads or one of ground line connection pads, the power supply and ground line connection pads being provided on a surface of a main semiconductor device. This feature is not disclosed by the cited IBM Technical Disclosure Bulletin.

### **CONCLUSION**

Claims 4-6, 11-13, and 16-19, which have been withdrawn from consideration since they were not elected in response to the Office Action mailed herein on July 15, 2002, have been cancelled, without prejudice or disclaimer, in order to reduce the amount of additional claim fees payable with this amendment. Applicant reserves the right to file Divisional Application(s) including claims 4-6, 11-13, and 16-19.

An earnest effort has been made to fully respond to the Examiner's objections.

In view of the above amendments it is believed that claims 1-3, 7-10, 14-15, 20-33 are in allowable condition.

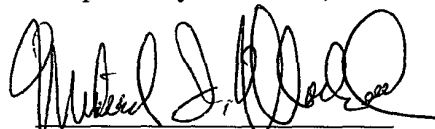
Attached hereto is a marked-up version of the changes made to the specification and the claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Please charge Deposit Account 50-1290 the sum of \$54.00 for three (3) claims added by this amendment in excess of the (20) claims covered by the basic filing fee.

Favorable consideration is most respectfully solicited.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



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Enclosure: Version With Markings to Show Changes Made

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**IN THE SPECIFICATION**

The paragraph at page 14, beginning from line 9, has been amended as follows:

[Fig. 1 is a] Fig. 1(a) and 1(b) are cross-sectional [view] views showing the condition of mounting of a semiconductor device according to a first embodiment of the present invention to a circuit board.

The paragraph beginning at page 15, line 1, has been amended as follows:

[Fig. 8 is a] Fig. 8(a) and 8(b) are cross-sectional [view] views showing the condition of a semiconductor device according to a second embodiment of the present invention mounted to a circuit board.

The paragraph beginning at page 17, line 16, has been amended as follows:

Specifically, a first embodiment of the present invention is described below, with references made to [Fig. 1 through] Figs. 1(a) and 1(b) to Fig. 7.

The paragraph beginning at page 19, line 4, has been amended as follows:

Fig. 3 and Fig. 6 show a flexible substrate 13 corresponding to the LSI device 1, Fig. 3 showing a flexible substrate corresponding to the LSI device of Fig. 2 and Fig. 6 showing a flexible substrate corresponding to the LSI device of Fig. 5. In both Fig. 3 and Fig. 6 a large number of metal foil leads 5 corresponding to either one of the power supply line connection pads 10 and ground line connection pads 11, are provided so as to extend outwardly from the

outside contour of the LSI device 1 on one surface of the insulation layer 3, and electrode pads 9 [is] are provided on the end part of the metal foil leads 5. Thus, only the insulation layer 3 exists in the center region of the LSI device 1, and the insulation layer 3 in this part has a large number of holes 12, of a diameter that just allows the passage of bumps, to be described below, corresponding to positions of the electrode pads 16 on the inside of the LSI device 1.

The paragraph beginning at page 20, line 1 has been amended as follows:

Fig. 4 and Fig. 7 show the condition in which decoupling capacitors 2 are mounted on the flexible substrate 13, Fig. 4 corresponding to Fig. 3, and Fig. 7 corresponding to Fig. 6. In both Fig. 4 and Fig. 7, decoupling capacitors are mounted so as to straddle across two neighboring metal foil leads 5, one metal foil lead 5 connected to a power supply line connection pad 10 of the LSI device 1 and one metal foil lead 5 connected to a ground line connection pad 11 of the LSI device 1. The decoupling capacitors 2 used in this case are chip capacitors, such as [a] laminated ceramic capacitors, tantalum capacitors, aluminum electrolytic capacitors, or organic capacitors or the like, which are mounted to the metal foil leads 5 by means of solder or conductive paste. Although the above-noted four types of chip capacitors can be used as the decoupling capacitors 2, laminated ceramic capacitors, which have small parasitic inductance and can provide a large capacitance, are suited for this use.

## **IN THE CLAIMS**

Claim 1 has been rewritten as follows:

1. (Once Amended) A semiconductor device comprising:

a main semiconductor device having on a circuit-formation surface a plurality of power supply line connection pads and a plurality of ground line connection pads, conductors each of which is electrically connected to either one of said power supply connection pads [and the] or one of said ground line connection pads, respectively; and

capacitors electrically connected to at least one surface of said conductors.